AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) A method for controlling a self refresh state of memory in a computer system, comprising:

supplying at least one memory control signal to the memory from a first integrated circuit in the computer system according to an operational state; and

supplying the memory control signal from another location in the computer system when the computer system is in a power savings state to maintain memory in the self refresh state, the other location in the computer system being independent of the first integrated circuit during normal operation.

2. (Original) The method as recited in claim 1 wherein the first integrated circuit is completely powered off during the power savings state.

3. (Original) The method as recited in claim 1 wherein the power savings state is a suspend to RAM state.

4. (Original) The method as recited in 1 wherein the memory control signal is a clock enable signal.

5. (Previously Presented) The method as recited in 1 wherein the memory control signal is a reset signal.

6. (Original) The method as recited in claim 4 wherein the clock enable signal is low while the memory is maintained in the self refresh state.

7. (Original) The method as recited in claim 1 wherein the memory control signal is held at a first value to keep the memory in the self refresh state.

8. (Canceled)

9. (Currently amended) A method for controlling a self refresh state of memory in a computer system, comprising:

controlling at least one memory control signal being supplied to the memory from a first integrated circuit in the computer system according to an operational state;

controlling the memory control signal from another location in the computer system when the computer system is in a power savings state to maintain memory in the self refresh state;

isolating the first integrated circuit from the memory during the power savings state; and

~~The method as recited in claim 8~~ wherein isolating further includes disabling a switch coupling the memory control signal from the first integrated circuit to the memory by driving a switch enable signal to a first predetermined value to turn off the switch, the switch enable signal being driven from the other location.

10. (Original) The method as recited in claim 9 further comprising driving a signal line which is coupled to the switch and is coupled to the memory control signal input to the memory to a predetermined logical level from the other location, during the power savings state to control the memory control signal and wherein the signal line is driven at a high impedance by the other location during the operational state.

11. (Original) The method as recited in claim 10 wherein the switch enable signal is at a second predetermined value to turn on the switch during the operational state.

12. (Original) The method as recited in claim 9 wherein the other location drives the signal line coupled to the switch and coupled to the memory control signal input to the memory before the switch enable signal is driven to the first predetermined value to turn off the switch and wherein the switch enable signal is driven to the second predetermined value to turn on the switch before the other location drives the signal at high impedance.

13. (Previously presented) The method as recited in claim 1 wherein the first integrated circuit drives the memory control signal at at least a first logical level during the operational state and the other location drives the memory control signal at a high impedance level during the operational state and wherein the first integrated circuit is powered off during

the power savings state and the other location drives the memory control signal at a second logical level during the power savings state, to keep the memory in the self refresh state.

14. (Previously presented) A computer system comprising:

a system memory capable of operating in a self refresh state, the system memory coupled to receive at least one memory control signal required to be held at a first value during the self refresh state;

a memory control circuit coupled to the system memory to provide at least one memory control signal during an operational state; and

a second circuit independent of the memory control circuit, coupled to cause the memory control signal to be at the first value during a power savings state.

15. (Original) The computer system as recited in claim 14 further comprising an isolation circuit coupled between the memory control circuit and the memory, the isolation circuit being coupled to receive the memory control signal from the memory control circuit and to selectably provide the memory control signal from the memory control circuit to the memory.

16. (Original) The computer system as recited in claim 15 wherein the second circuit is coupled to provide a high impedance on an output terminal, during an operational state of the computer system, the output terminal being coupled to the isolation circuit and the memory to provide the memory control signal, and wherein the second circuit is coupled to drive the output terminal and thereby the memory control signal to a low voltage level during the power savings state.

17. (Previously Presented) The computer system as recited in claim 15 wherein the second circuit is coupled to provide an isolation control signal to the isolation circuit during the power savings state to isolate the memory control signal provided from the memory control circuit from the memory, during the power savings state.

18. (Original) The computer system as recited in claim 14 wherein the second circuit is coupled to provide a high impedance on an output terminal that is coupled to the memory control signal during an operational state of the computer system and wherein the second circuit

provides a logical level on the output terminal to drive the memory control signal to the first value during the power savings state.

19. (Original) The computer system as recited in claim 14 wherein the power savings state is a suspend to RAM state wherein system context is stored in the system memory during the suspend to RAM state.

20. (Original) The computer system as recited in claim 14 wherein the memory control circuit is on an integrated circuit having multiple power planes and all power planes are powered down during the power savings state.

21. (Currently amended) A computer system comprising:

first means for controlling system memory during an operational state; and

second means, for controlling the system memory during a power savings state to maintain the system memory in a self refresh state when the first means is ~~completely~~ powered off, the second means including means for holding an output terminal at a high impedance during the operational state and means for providing a first logic level through the output terminal during the power savings state, the output terminal being coupled to supply a control value at the first logic level to maintain the system memory in the self refresh state when the first means is powered off.

22. (Original) The computer system as recited in claim 21 further comprising isolation means to isolate the first means from the system memory during the power savings state.

23. (Original) The computer system as recited in claim 21 wherein the first and second means are disposed on one integrated circuit.

24. (Original) An integrated circuit of a computer system comprising:

a first output terminal for coupling to a memory control signal that is held at a first logic level to keep a memory in a self refresh state, the integrated circuit responsive to a first operational state of the computer system to place the output terminal at a high

impedance level and responsive to a power savings state in the computer system to supply the first logic level on the output terminal.

25. (Original) The integrated circuit as recited in claim 24 further comprising a second output terminal for coupling to a switch, the integrated circuit responsive to the first operational state of the computer system to place the second output terminal at a logic level causing the switch to pass through a memory control signal coupled to the switch and responsive to the power savings state to supply a different logic level at the output terminal, the second logic level causing the switch to not pass through the memory control signal.

26. (Previously presented) A method for controlling a self refresh state of a memory in a computer system, comprising:

controlling at least one memory control signal being supplied to the memory from a first region in an integrated circuit in the computer system during an operational state;

controlling the at least one memory control signal from another location in the integrated circuit during a power savings state in which the first region is not powered, to maintain memory in the self refresh state;

wherein the memory control signal is held at a first value to keep the memory in the self refresh state; and

wherein an asserted reset signal holds the memory control signal at the first value in the first integrated circuit during the power savings state.

27. (Original) The method as recited in claim 26 wherein the power savings state is a an S3 suspend to RAM state.

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Previously Presented) An apparatus comprising:

a memory control circuit coupled to control at least one memory control signal during an operational state; and

a second circuit coupled to cause the memory control signal to be at a logic level to maintain a memory in a self refresh state, the second circuit being operational during a power savings state in which power to the memory control circuit is turned off, wherein a reset signal coupled to the second circuit, when asserted, causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state.

32. (Original) The apparatus as recited in claim 31 wherein the memory control circuit and the second circuit are disposed on one integrated circuit.

33. (Original) The apparatus as recited in claim 32 wherein the integrated circuit includes the memory control circuit and a central processing circuit (CPU).

34. (Canceled)